Amendments to the Drawings

FIG. 1 has been amended to change "passive action layer" to "passivation layer" as indicated in the mark-up version of FIG. 1 attached as an Appendix. A replacement sheet for FIG. 1 with the requested change is also attached.

REMARKS

Status of Claims

In the Office Action, Claims 1-15 and 17-19 were noted as pending in the application and all claims were rejected under 35 U.S.C. 103(a). In addition, FIG. 1 was found objectionable.

By the present Amendment, Claims 1, 12, 17 and 19 have been amended, and Claim 11 has been canceled so that Claims 1-10, 12-15 and 17-19 remain pending in the subject application. FIG. 1 has been amended, and a replacement sheet has been attached to this response.

The claim rejections and drawing objection are addressed below.

Objection to the Drawings

On page 2, item 1 of the Office action, FIG. 1 was found objectionable for stating "passive action layer" rather than "passivation layer." The attached replacement sheet overcomes the objection. Entry of the replacement sheet in the subject application and withdrawal of the objection are requested.

Rejection of Claims 1- 9, 12, 13 and 17 under 35 U.S.C. § 103(a) based on Suzuki (U.S. Patent No. 6,469,315 B1) in view of Wolter (U.S. Patent No. 4,677,457)

On page 3, item 3 of the Office action, Claims 1-9, 12, 13 and 17 were rejected under 35 U.S.C. § 103(a) based on Suzuki (U.S. Patent No. 6,469,315 B1) in view of Wolter (U.S. Patent No. 4,677,457). For reasons already made of record, it is submitted that Claims 1-9, 12, 13 and 17 are patentable over the cited prior art. Claim 16 has been canceled because its limitations have been incorporated into Claim 1.

Claim 1 has been amended to recite additional features not disclosed in Suzuki and Wolter. Claim 1 as amended is restated below for the Examiner's convenience:

> 1. (currently amended) A high electron mobility transistor (HEMT) comprising:
>
> a channel layer being composed of a II-VI compound semiconductor zinc oxide;
>
> **a gate contact disposed [[on]] <u>in proximity to, but not in contact with,</u> said channel layer**; and

> a gate insulating layer disposed between and in contact with said gate contact and said channel layer and composed of at least one of a Group-III nitride compound semiconductor and a magnesium zinc oxide (MgZnO) quantum well structure, **said gate insulating layer having side walls, said gate contact positioned between the sidewalls of said gate insulating layer so that sides of said gate contact face the side walls of said gate insulating layer**.

Support for these amendments is found in FIG. 1 and Paragraphs [0009]-[0011] and [0017]-[0020], for example. In Suzuki, the barrier layer 17 is not in contact with either the channel layer 13 or the gate electrode 21. Thus, structurally, Suzuki does not disclose the claimed limitation "**a gate insulating layer disposed between and in contact with said gate contact and said channel layer**" recited in Claim 1 as amended. Moreover, Claim 1 has been amended to recite "**said gate insulating layer having side walls, said gate contact positioned between the sidewalls of said gate insulating layer so that sides of said gate contact face the side walls of said gate insulating layer**." Neither Suzuki nor Wolter disclose this feature of the claimed invention, nor do they include any teaching or suggestion as to how their disclosures could be modified or combined to obtain the claimed structure. Murota (cited against Claim 11, now canceled) also fails to disclose this feature of the claimed invention because it does not include side walls of a gate insulating layer with the claimed compositions in relation to the channel layer and gate contact of the claimed composition. Accordingly, it is submitted the Claim 1 as amended is patentable over the prior art of record.

Claims 2-9, 12, 13, and 16 depend from Claim 1 as amended and thus include all of the limitations of the Claim. Accordingly, the amendments to independent Claim 1 overcome the rejection of these Claims as well.

Claim 17 as amended is restated for the Examiner's convenience as follows:

> 17. (currently amended) A method comprising the steps of:
>
> defining a channel layer composed of a II-VI compound semiconductor zinc oxide;

forming a gate insulating layer in contact with said channel layer and composed of at least one of a Group-III nitride compound semiconductor and a magnesium zinc oxide (MgZnO) quantum well structure, said gate insulating layer formed with side walls; and

forming a gate contact disposed on and in contact with said gate insulating layer and positioned between said side walls, said gate contact formed to have sides facing said side walls of said gate insulating layer, said gate contact formed in proximity to, but not in contact with, said channel layer.

Support for these amendments is found in FIG. 1 and Paragraphs [0009]-[0011] and [0017]-[0020], for example. Suzuki does not disclose any step of "**forming a gate insulating layer on and in contact with said channel layer**" as recited in Claim 17 since Suzuki's barrier layer 17 and channel layer 13 are not in contact, but instead are separate. Furthermore, neither Suzuki nor Wolter disclose "**said gate insulating layer formed with side walls**" and "**forming a gate contact disposed on and in contact with said gate insulating layer and positioned between said side walls, said gate contact formed to have sides facing respective side walls of said gate insulating layer, said gate insulating layer positioned in proximity to, but not in contact with, said channel layer**" as recited in Claim 17 as amended. Neither Suzuki nor Wolter disclose this limitation, whether considered alone or in combination, nor is there any disclosure in the prior art suggesting modification in any way that would meet all of the limitations of Claim 17. Murota (cited against Claim 11, now canceled) also fails to disclose this feature of the claimed invention because it does not disclose forming side walls of a gate insulating layer with the claimed compositions in combination with steps of forming the channel layer and gate contact of the claimed composition. Accordingly, it is submitted that Claim 17 as amended is patentable over the prior art of record.

Rejection of Claim 10 under 35 U.S.C. § 103(a) based on Suzuki (U.S. Patent No. 6,469,315 B1) in view of Wolter (U.S. Patent No. 4,677,457) in further view of Shanfield (U.S. Patent No. 5,880,483)

On page 4, item 4 of the Office action, Claim 10 was rejected under 35 U.S.C. 103(a) based on Suzuki, Wolter and Shanfield. Shanfield is relied upon as disclosing a passivation layer 36 on a gate electrode 24, source electrode 20, and drain electrode 22.

It is submitted that there is no teaching or suggestion in Suzuki, Wolter or Shanfield that would have led the person of ordinary skill in the art to combine these citations as done in the Office action. Accordingly, impermissible hindsight has been used in which the Applicant's disclosure, not the prior art, has been used as the basis to provide the motivation to modify or combine the citations. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988).

In addition, Claim 10 depends from Claim 1 as amended and therefore includes all of the limitations of that Claim. Because Shanfield fails to disclose the deficiencies of Suzuki and Wolter as noted above with respect to Claim 1, Applicant submits that Claim 10 is patentable over the prior art of record due at least to its dependency from Claim 1. Thus, for at least the reasons stated above with respect to Claim 1 as amended, Applicant submits that Claim 10 is patentable over the prior art or record.

Rejection of Claim 11 under 35 U.S.C. § 103(a) based on Suzuki (U.S. Patent No. 6,469,315 B1) in view of Wolter (U.S. Patent No. 4,677,457) in further view of Murota (U.S. Published Appl. No. US2002/0109135 A1)

On page 5, item 5 of the Office action, Claim 11 was rejected under 35 U.S.C. 103(a) based on Suzuki, Wolter and Murota. By the present Amendment, Claim 11 has been canceled from the subject application so that the rejection of this Claim is moot.

Rejection of Claim 14, 15 and 19 under 35 U.S.C. § 103(a) based on Suzuki (U.S. Patent No. 6,469,315 B1) in view of Wolter (U.S. Patent No. 4,677,457) in further view of Nishikawa et al. (U.S. Patent No. 6,323,053)

On page 5, item 6 of the Office action, Claims 14, 15, and 19 were rejected under 35 U.S.C. 103(a) based on Suzuki in view of Wolter, in further view of Nishikawa. Nishikawa is relied upon to disclose a ZnO substrate with a c-surface.

It is submitted that there is no teaching or suggestion in the prior art that would have led the person of ordinary skill in the art to combine Suzuki, Wolter or Nishikawa as done in the

Office action. Accordingly, impermissible hindsight has been used in which the Applicant's disclosure, not the prior art, has been used as the basis to provide the motivation to modify or combine the citations. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988).

The Office action cites *In re Leshin*, 277 F.2d 197 (C.C.P.A. 1960) for the proposition that to select a known material on the basis of its suitability for the intended use of the claimed device is a matter of obvious design choice. However, with reference to FIG. 4, Nishikawa discloses a structure with a c-surface ZnO substrate 11, a terminating hydrogen layer 12, a gallium selenide (GaSe) layer 13, a nitrogen-substituted buffer layer 23, and a gallium nitride (GaN) layer 14. The purpose of this complex structure of intervening layers 12, 13, 14 between the GaN layer 14 and the ZnO substrate 11 is to relax the stress between them due to lattice mismatch. It does not disclose the desirability of providing a ZnO channel layer on a ZnO substrate, on which is formed either a Group III nitride compound semiconductor or a magnesium zinc oxide (MgZnO) quantum well structure, as claimed in Claims 14, 15 and 19. In the case of the channel layer being a Group III nitride compound semiconductor, the pseudomorphic strain between the ZnO channel layer supported by the ZnO structure is what produces the two-dimensional electron gas of the semiconductor device. Nishikawa "teaches away" from this configuration, instead instructing that one must use layers 12, 13, 14 to relax strain between the nitride and layers. This would reduce effectiveness or lead to inoperability of the claimed device. As to the case in which the channel layer is composed of a MgZnO quantum well structure, neither Nishikawa nor any other citation discloses MgZnO, let alone a quantum well structure made with it. Thus, *In re Leshin* is inapposite here: the material of the cited art, namely c-surface ZnO, is not used being use for the intended purpose of the claimed invention.

In addition, Claims 14 and 15 depend from Claim 1 as amended and therefore includes all of the limitations of that Claim. Because Nishikawa fails to disclose the deficiencies of Suzuki and Wolter as noted above with respect to Claim 1, Applicant submits that Claim 11 is patentable over the prior art of record due to its dependency from Claim 1.

Claim 19 depends from Claim 17 and includes all limitations of that Claim. Because the Nishikawa fails to disclose the deficiencies of Suzuki and Wolter as noted above with respect to

Claim 17, Applicant submits that Claim 19 is patentable over the prior art of record due to its dependency from Claim 17.

Rejection of Claim 18 under 35 U.S.C. § 103(a) based on Suzuki (U.S. Patent No. 6,469,315 B1) in view of Wolter (U.S. Patent No. 4,677,457) in further view of Ando (U.S. Patent No. 6,429,467 B1)

On page 7, item 6 of the Office action, Claim 18 was rejected under 35 U.S.C. 103(a) based on Suzuki in view of Wolter, in further view of Ando. Ando is relied upon to disclose a gate insulating layer formed by metal organic chemical vapor deposition (MOCVD). However, Claim 18 recites that "...the gate insulating layer is formed by metal organic chemical vapor deposition (MOCVD)." 35 U.S.C. 103(a) requires that the claim be considered as a whole, not in piecemeal fashion. Due to the other claim limitations, Claim 18 effectively recites using MOCVD to form a gate insulating layer composed of Group III nitride compound semiconductor or a magnesium zinc oxide (MgZnO) quantum well structure, in contact with a ZnO channel layer. Ando does not disclose use of MOCVD in the claimed manner. Therefore, Applicant submits Claim 18 is patentable over the prior art of record.

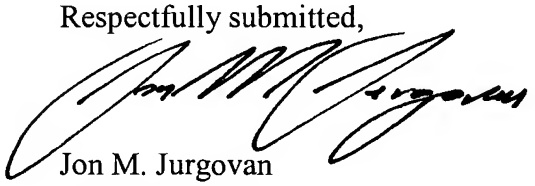
Furthermore, Claim 18 depends from Claim 17 and thus includes all of the limitations of that Claim. Because Ando fails to disclose the deficiencies of Suzuki and Wolter as noted above with respect to Claim 17, it is submitted that Claim 18 is patentable over the prior art of record.

Conclusion

It is submitted that FIG. 1 has been amended as necessary to overcome the objection. Also, it is submitted that Claims 1-10, 12-15, and 17-19 have been amended as necessary to overcome the rejections under 35 U.S.C. 103(a). Accordingly, reconsideration of the drawings and Claims as amended, withdrawal of the objection and rejections, and a Notice of Allowance for all pending Claims, are earnestly solicited.

It is not believed that extensions of time or fees for net addition of claims are required, beyond those that may otherwise be provided for in documents accompanying this paper. However, in the event that additional extensions of time are necessary to allow consideration of this paper, such extensions are hereby petitioned under 37 CFR § 1.136(a), and any fee required therefore (including fees for net addition of claims) is hereby authorized to be charged to Deposit Account No. 16-0605.

Respectfully submitted,



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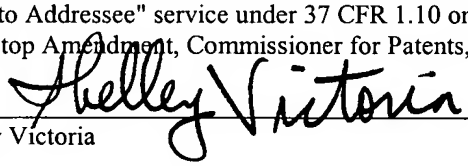

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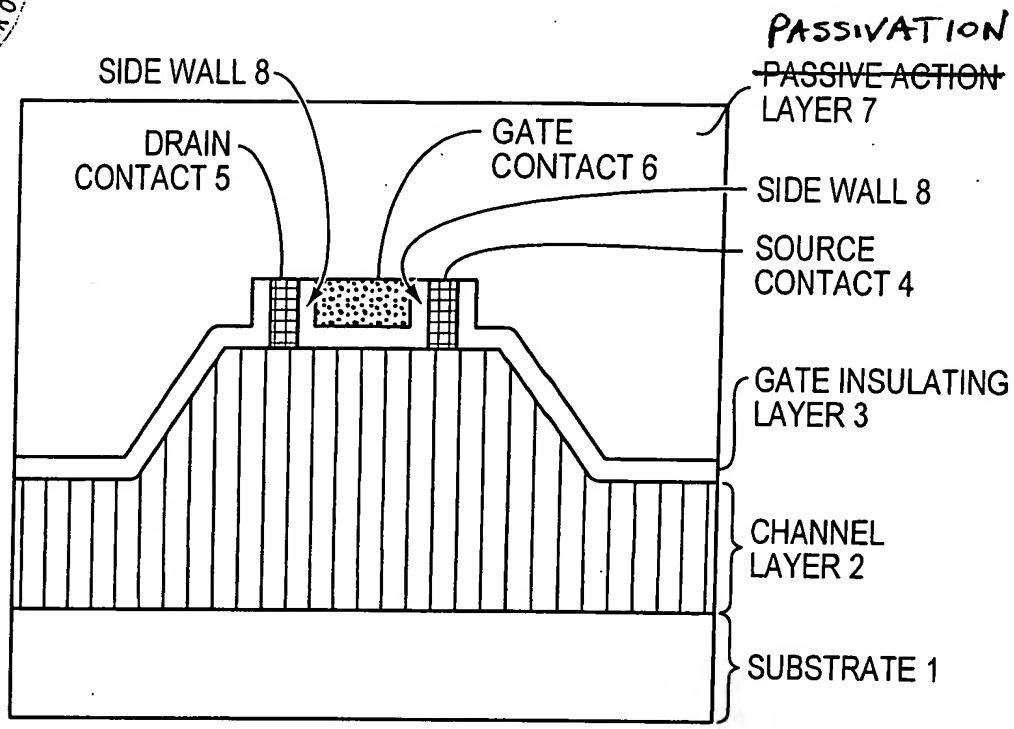

FIG. 1